

WHAT IS CLAIMED IS:

1. A bipolar transistor, comprising:

a substrate having a collector region of a first conductivity type;

5 a base layer of a single crystalline structure and including impurities of a second conductivity type located over the collector region;

10 an emitter region defined at least in part by impurities of the first conductivity type contained in the base layer; and

15 an emitter electrode of the first conductivity type contacting the emitter region, wherein at least a portion of the emitter electrode which is in contact with the emitter region has a single crystalline structure.

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2. The bipolar transistor of claim 1, further comprising a base electrode located over the base region.

20 3. The bipolar transistor of claim 2, wherein the base electrode comprises at least one of polysilicon and polysilicon-germanium.

4. The bipolar transistor of claim 1, further comprising a metal layer formed on the emitter electrode.

5. The bipolar transistor of claim 4, wherein at least of portion of the emitter electrode in contact with the metal layer has a single crystalline structure.

5 6. The bipolar transistor of claim 1, further comprising a metal layer formed on the base layer.

7. The bipolar transistor of claim 2, further comprising a metal layer formed on the base electrode.

10 8. The bipolar transistor of claim 4, wherein the metal layer is a silicide layer, and wherein the bipolar transistor further comprising a metal electrode layer contacting the silicide layer.

15 9. The bipolar transistor of claim 1, wherein at least a portion of the emitter electrode not in contact with the emitter region has a polycrystalline or amorphous structure.

20 10. The bipolar transistor of claim 1, wherein an entirety of the emitter electrode has a single crystalline structure.

11. The bipolar transistor of claim 4, wherein at least a portion of the emitter electrode in contact with the metal layer has a polycrystalline or amorphous structure.

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12. The bipolar transistor of claim 1, wherein an impurity concentration of the emitter electrode varies in a depth direction.

10 13. The bipolar transistor of claim 12, wherein an upper portion of the emitter electrode has a higher impurity concentration than a lower portion of the emitter electrode.

15 14. The bipolar transistor of claim 1, wherein the emitter electrode comprises one of Si, SiGe or a composite of Si and SiGe.

20 15. The bipolar transistor of claim 1, further comprising a base region located in a surface of the collector region and below the base layer.

16. The bipolar transistor of claim 2, further comprising a sidewall spacer which electrically insulates the emitter electrode from the base electrode.

5 17. A bipolar transistor, comprising:

a substrate having a collector region of a first conductivity type;

a base region of a single crystalline structure and of a second conductivity type located over the collector 10 region;

an emitter region defined at least in part by impurities of the first conductivity type contained in the base layer; and

an emitter electrode comprising an epitaxially grown 15 layer of the first conductivity type contacting the emitter region.

18. The bipolar transistor of claim 17, wherein the epitaxially grown layer was grown at a temperature of 20 less than 900°C.

19. The bipolar transistor of claim 17, further comprising a silicide layer formed on the epitaxially

grown layer of the emitter electrode, and a metal electrode layer formed on the silicide layer.

20. The bipolar transistor of claim 19, further
5 comprising a metal electrode layer formed on the epitaxially grown layer of the emitter electrode.

21. The bipolar transistor of claim 17, wherein the emitter electrode further comprises a polycrystalline
10 grown layer formed over the epitaxially grown layer.

22. The bipolar transistor of claim 21, wherein an interface between the epitaxially grown layer and the polycrystalline grown layer is structurally characterized
15 by both layers being continuously grown in the absence of a vacuum break.

23. The bipolar transistor of claim 22, wherein a structural transition from the epitaxially grown layer to
20 polycrystalline grown layer of the emitter electrode is gradual.

24. The bipolar transistor of claim 23, further comprising a silicide layer formed on the polycrystalline

grown layer of the emitter electrode, and a metal electrode layer formed on the silicide layer.

25. The bipolar transistor of claim 24, further
5 comprising a metal electrode layer formed on the polycrystalline grown layer of the emitter electrode.

26. The bipolar transistor of claim 17, wherein the
emitter electrode further comprises an amorphous layer
10 formed over the epitaxial layer.

27. The bipolar transistor of claim 17, further
comprising an insulating layer formed on the substrate
and having a through hole aligned over the emitter
15 region, wherein the epitaxial layer is at least partially
contained in the through hole.

28. The bipolar transistor of claim 27, wherein the
epitaxial layer extends over a top surface of the
20 insulating layer.

29. The bipolar transistor of claim 17, wherein the
epitaxially grown layer comprises one of Si, SiGe or a
composite of Si and SiGe.

30. The bipolar transistor of claim 21, wherein the epitaxially grown layer and the polycrystalline grown layer comprise one of Si, SiGe or a composite of Si and
5 SiGe.

31. A method for forming an emitter contact of a bipolar transistor, comprising:

10 growing an emitter electrode layer containing an impurity of a first conductivity type over the surface of a base layer of a second conductivity type, wherein at least a portion of the emitter electrode layer in contact with the base layer is grown having a single crystalline structure;

15 forming an emitter region of the first conductivity type in the base layer; and

forming a metal layer on the emitter electrode layer.

20 32. The method of claim 31, wherein the metal layer is a silicide layer, and wherein the method further comprises forming a metal contact layer on the silicide layer.

33. The method of claim 31, wherein an entirety of the emitter electrode layer is grown having the single crystalline structure.

5 34. The method of claim 31, wherein an entirety of the emitter electrode layer is grown in the absence of a vacuum break.

10 35. The method of claim 31, wherein a portion of the emitter electrode layer not in contact with the base layer is grown having a polycrystalline structure.

15 36. The method of claim 35, wherein an entirety of the emitter electrode layer is grown in the absence of a vacuum break.

20 37. The method of claim 36, wherein the emitter electrode is grown such that a structural transition from the single crystalline portion to polycrystalline portion of the emitter electrode layer is gradual.

38. The method of claim 31, wherein a portion of the emitter electrode layer not in contact with the base layer is formed having an amorphous structure.

39. The method of claim 31, wherein the emitter electrode layer comprises one of Si, SiGe or a composite of Si and SiGe.

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40. The method of claim 31, wherein growing the emitter electrode layer comprises epitaxial growth at a temperature of less than 900°.

10 41. The method of claim 31, wherein the emitter region is formed by diffusion of impurities from the emitter electrode layer into the base layer.

15 42. The method of claim 31, wherein the emitter region is formed by ion implantation prior to growing the emitter electrode layer.

20 43. The method of claim 31, further comprising forming the emitter electrode layer such that an impurity concentration of the emitter electrode layer varies in a depth direction.

44. The method of claim 31, further comprising forming an upper portion of the emitter electrode layer

with a higher impurity concentration than a lower portion of the emitter electrode layer.

45. A method of forming a bipolar transistor,
5 comprising:

forming a collector region of a first conductivity type in a substrate;

10 forming a base layer, including growing a first epitaxial layer of a second conductivity type over an upper surface of the substrate;

forming an emitter electrode layer over the base layer, including growing a second epitaxial layer containing an impurity of the first conductivity type from an upper surface of the first epitaxial layer; and

15 diffusing the impurity from the second epitaxial layer into the first epitaxial layer to form an emitter region of the first conductivity type in the first epitaxial layer;

20 forming a metal layer on the emitter electrode layer.

46. The method of claim 45, wherein the metal layer is a silicide layer, and wherein the method further

comprises forming a metal contact layer on the silicide layer.

47. The method of claim 45, wherein the second
5 epitaxial layer is grown at a temperature of less than
900°C.

48. The method of claim 45, wherein an entirety of
the emitter electrode layer is constituted by the second
10 epitaxial layer.

49. The method of claim 45, wherein an entirety of
the emitter electrode layer is formed in the absence of a
vacuum break.

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50. The method of claim 45, wherein forming the
emitter electrode layer further includes growing a
polycrystalline layer over the second epitaxial layer.

20 51. The method of claim 50, wherein the metal layer
is formed on the polycrystalline layer.

52. The method of claim 50, wherein an entirety of the emitter electrode layer is grown in the absence of a vacuum break.

5 53. The method of claim 52, wherein the emitter electrode is grown such that a structural transition from the second epitaxial layer to polycrystalline layer of the emitter electrode layer is gradual.

10 54. The method of claim 45, wherein a portion of the emitter electrode layer not in contact with the base layer is formed having an amorphous structure.

15 55. The method of claim 45, wherein the emitter electrode layer comprises one of Si, SiGe or a composite of Si and SiGe.